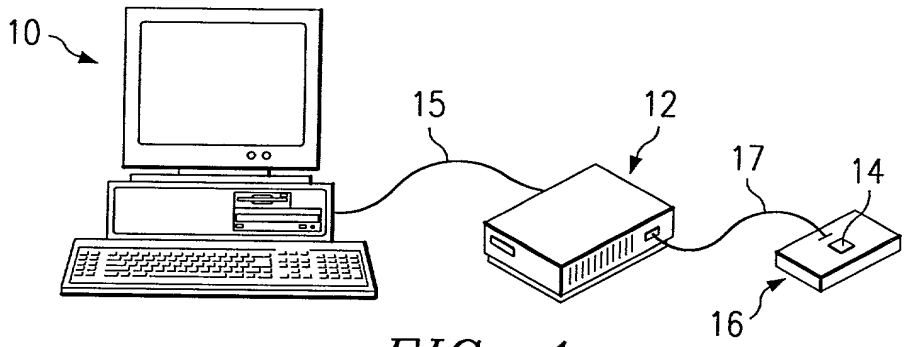
10
15
12
17
14
16

FIG. 1

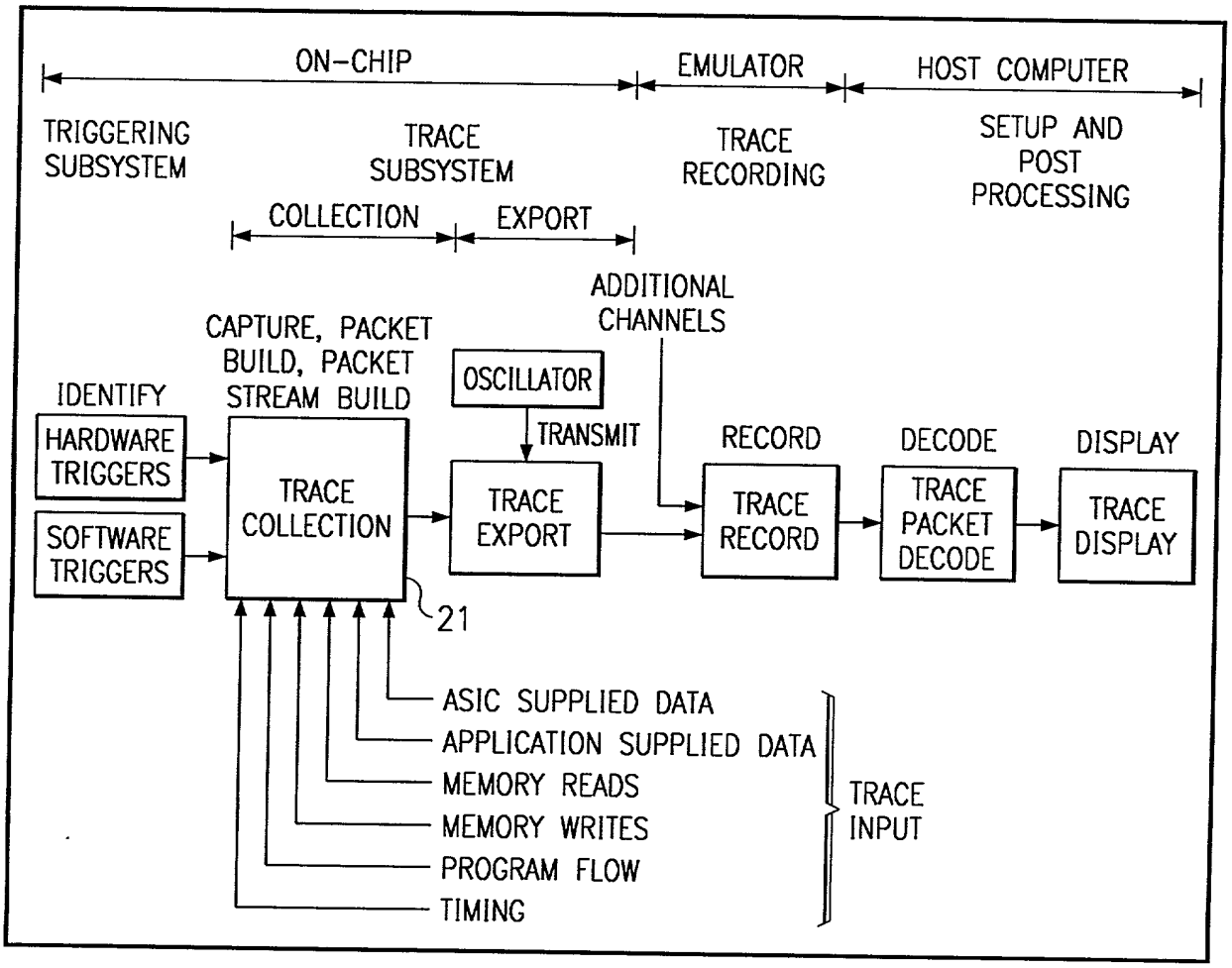
ON-CHIP
EMULATOR
HOST COMPUTER
TRIGGERING SUBSYSTEM
TRACE SUBSYSTEM
TRACE RECORDING
SETUP AND POST PROCESSING
COLLECTION
EXPORT
ADDITIONAL CHANNELS
CAPTURE, PACKET BUILD, PACKET STREAM BUILD
OSCILLATOR
IDENTIFY
HARDWARE TRIGGERS
SOFTWARE TRIGGERS
TRACE COLLECTION
TRANSMIT
TRACE EXPORT
RECORD
TRACE RECORD
DECODE
TRACE PACKET DECODE
DISPLAY
TRACE DISPLAY
21
ASIC SUPPLIED DATA
APPLICATION SUPPLIED DATA
MEMORY READS
MEMORY WRITES
PROGRAM FLOW
TIMING
TRACE INPUT

FIG. 2

OPCODE	COMMAND MEANING
00 0000 0000	NO INFORMATION
00 0000 0001	RESERVED
00 0000 0010	PC TRACE GAP
00 0000 0011	REPEAT INSTRUCTION
00 0000 0100	COUNTER START
00 0000 0101	COUNTER OVERFLOW/COUNTER VALUE
00 0000 0110	RESERVED
00 0000 0111	COMMAND ESCAPE
00 0000 1xxx	EXCEPTION OCCURRED
00 0001 0xxx	TIMING SYNC POINT
00 0001 1xxx	MEMORY REFERENCE SYNC POINT
00 0010 xxxx	PC SYNC POINT/FIRST/LAST/TRIGGER
00 010x xxxx	SAME PC
00 011x xxxx	CPU AND ASIC DATA
00 10xx xxxx	RESERVED
00 11xx xxxx	MEMORY REFERENCE BLOCK
01 xxxx xxxx	BRANCH/BEGINNING OF PARAMETER
10 xxxx xxxx	CONTINUE
11 xxxx xxxx	TIMING

FIG. 3

TIMING PACKET EXAMPLES

OPCODE	CYCLE BITS	MEANING
11	00000000	8 CONSECUTIVE CYCLES OF EXECUTION
11	11111111	8 CONSECUTIVE STALL CYCLES
11	11110000	THE RIGHT MOST BITS INDICATE THE PROCESSOR EXECUTED FOR 4 CYCLES AND THEN STALLED 4 CYCLES
11	10101010	THE BITS MEAN EXECUTE, STALL, EXECUTE, STALL, EXECUTE, STALL, EXECUTE, STALL, EXECUTE, AND STALL RESPECTIVELY

FIG. 4

TIMING SYNC PACKET

TIMING SYNC HEADER	3-BIT PC SYNC ID

FIG. 5

PC SYNC POINT TYPES

TYPE	SYNC TYPE	REASON FOR SYNC POINT
000	TRIGGER	USER DEFINED TRIGGER
001	FIRST POINT	STANDBY MODE
010	SYNC POINT	PERIODICALLY GENERATED
011	FIRST POINT	STREAM ENABLED
100	LAST POINT	STREAM DISABLED

FIG. 6

TIME

PC SYNC POINT

OPCODE			
00 0010		TYPE (3 BITS)	RESERVED
10	SYNC ID (3 BITS)	RESERVED	TIME INDEX (3 BITS)
10	CURRENT		LSB
10	PC		
10	ABSOLUTE		
10	MSB	ADDRESS	

OPCODES

FIG. 7

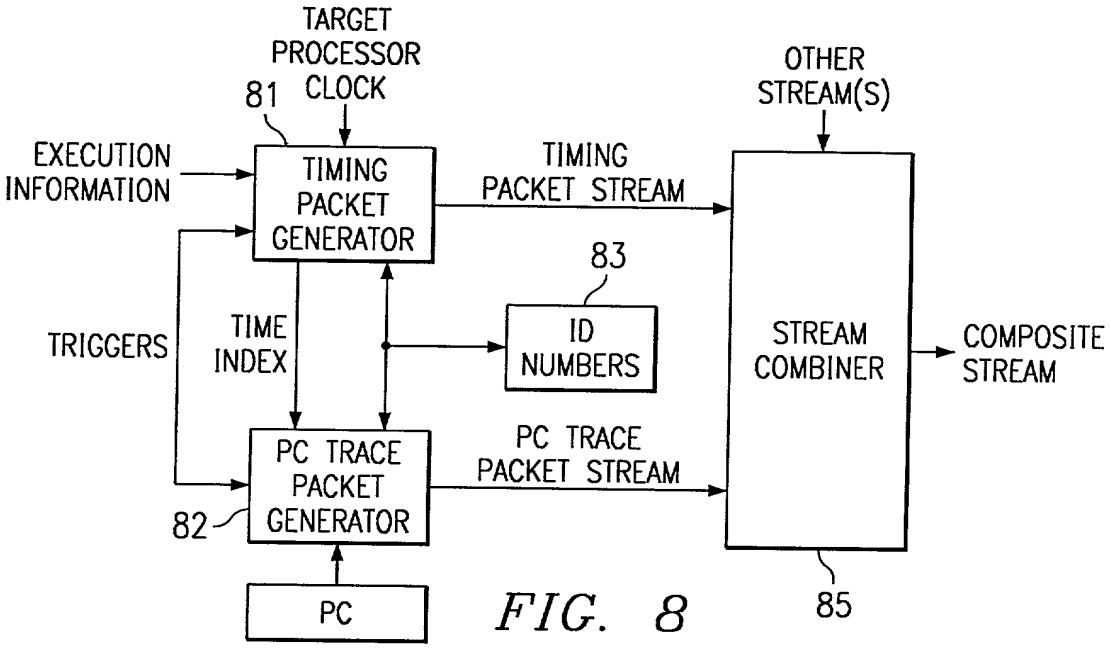

FIG. 8

TIME ↓

PACKET SEQUENCE			
0011		LD/ST (1 BIT)	DATA, ADDRESS, PC (5 BITS)
01	DATA BYTE 0 LSB		
10	DATA BYTE 1		
10	DATA BYTE 2		
10	DATA BYTE 3		
10	DATA BYTE 4		
10	DATA BYTE 5		
10	DATA BYTE 6		
10	MSB DATA BYTE 7		
01	DATA ADDRESS BYTE 0 LSB		
10	DATA ADDRESS BYTE 1		
10	DATA ADDRESS BYTE 2		
10	MSB DATA ADDRESS BYTE 3		
01	NATIVE PC ADDRESS BYTE 0 LSB	OR	OFFSET, BITS 7-0 (8 BITS)
10	NATIVE PC ADDRESS BYTE 1		OFFSET, BITS 15-8 (8 BITS) (OPTIONAL)
10	NATIVE PC ADDRESS BYTE 2		NOT NEEDED
10	MSB NATIVE PC ADDRESS BYTE 3		NOT NEEDED

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OPCODES

FIG. 9

MEMORY REFERENCE SYNC POINT

OPCODE	PARAMETER FIELD (3-BITS)
00 00011	MSB SYNC ID LSB

FIG. 10

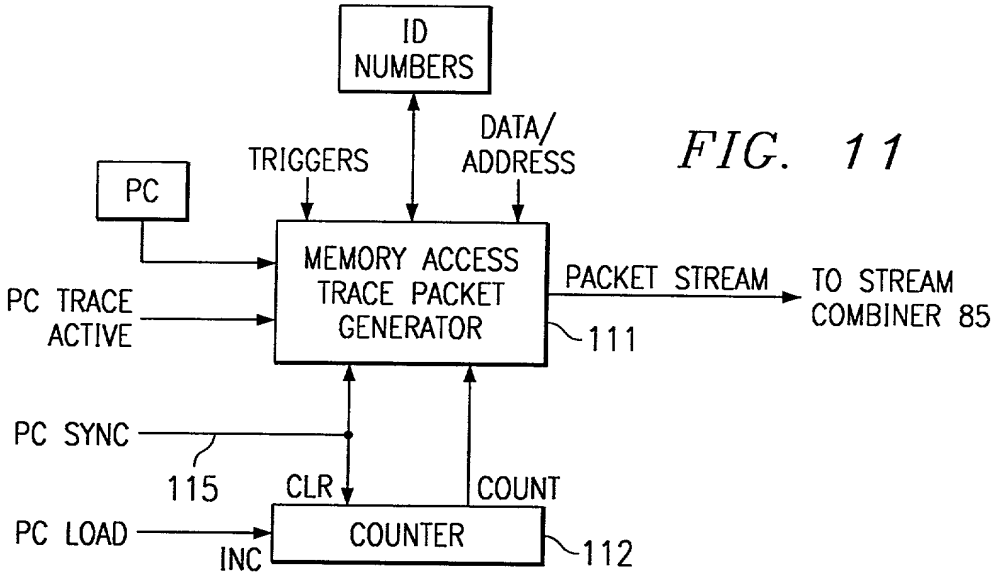


FIG. 11

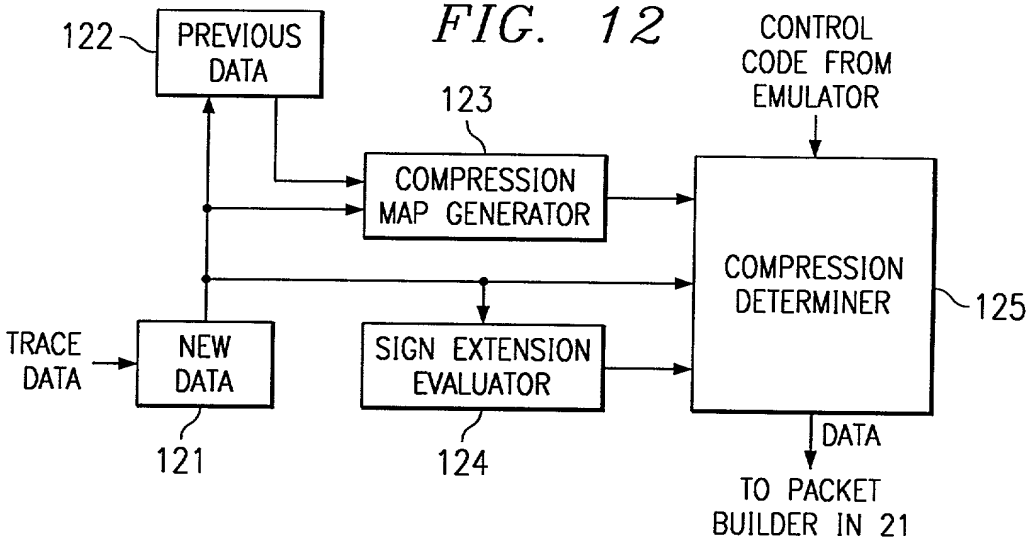
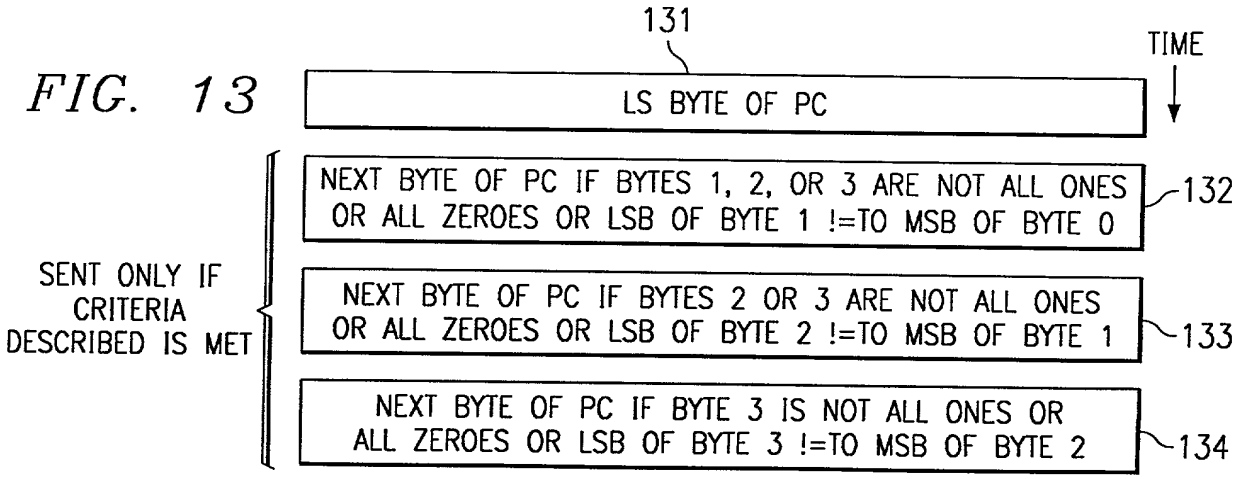


FIG. 12

FIG. 13



COMPRESSION EXAMPLE 0		
PREVIOUS DATA		11111111 11111111 11111111 10000011
NEW DATA		11111111 11111111 11111111 10000011
COMPRESSION BIT MAP SENT		NONE BECAUSE ONLY ONE BYTE COMPRESSES
SEND BYTES		DROPPED DROPPED DROPPED SENT
		BYTE #0 IS SENT

FIG. 14

COMPRESSION EXAMPLE 1		
PREVIOUS DATA		11111111 11111111 11111111 10000011
NEW DATA		11111111 11111111 11111111 10000100
COMPRESSION BIT MAP SENT		NO BECAUSE ONLY ONE BYTE COMPRESSES
SEND BYTES		DROPPED DROPPED DROPPED SENT
		BYTE #0 IS SENT

FIG. 15

COMPRESSION EXAMPLE 2		
PREVIOUS DATA		11101111 11101111 11101111 10000011
NEW DATA		11101111 11101111 11101111 10000100
COMPRESSION BIT MAP SENT		YES BECAUSE NO SIGN EXTENSION AND TWO OR MORE BYTES COMPRESS
SEND BYTES		DROPPED DROPPED DROPPED SENT
		BYTE #0 IS SENT

FIG. 16

COMPRESSION EXAMPLE 3		
PREVIOUS DATA		00001000 01111110 11000011 10000100
NEW DATA		11111111 11111111 11000011 10000100
COMPRESSION BIT MAP SENT		YES BECAUSE NO SIGN EXTENSION AND TWO OR MORE BYTES COMPRESS
SEND BYTES		DROPPED DROPPED DROPPED DROPPED
		NO BYTES ARE SENT

FIG. 17

COMPRESSION EXAMPLE 4		
PREVIOUS DATA		10000011 00000100 11111111 11111111
NEW DATA		11111111 11111111 11111111 11111111
COMPRESSION BIT MAP SENT		YES BECAUSE TWO OR MORE BYTES NOT COVERED BY SIGN EXTENSION COMPRESS
SEND BYTES		DROPPED DROPPED DROPPED DROPPED
		NO BYTES ARE SENT

FIG. 18

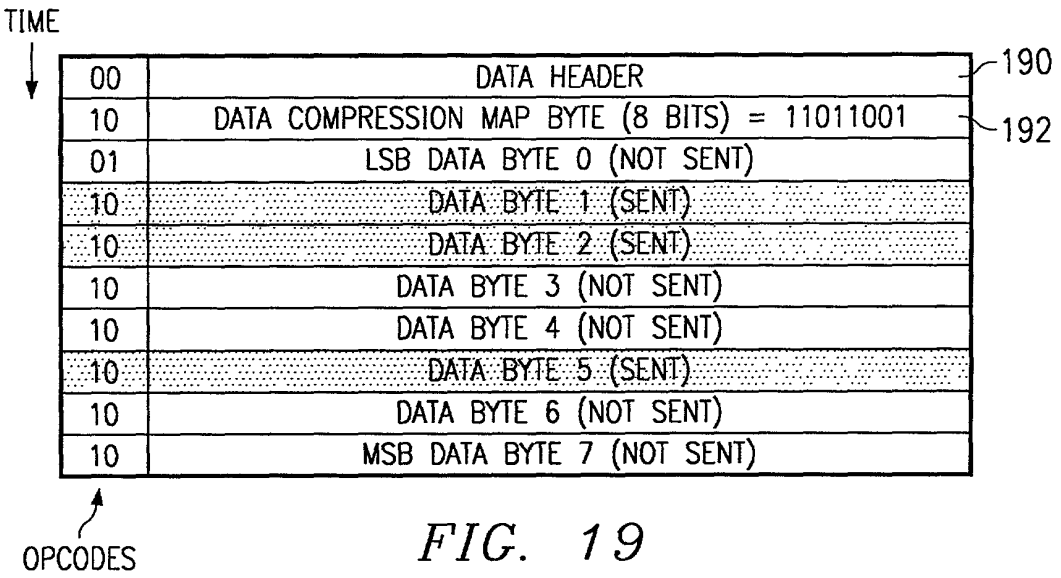


FIG. 19

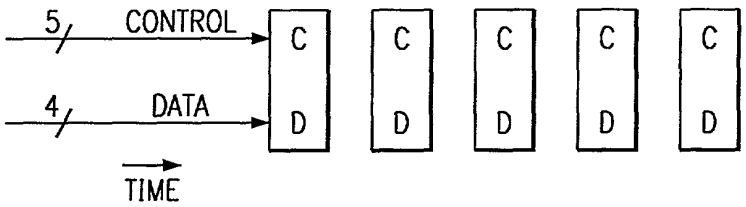


FIG. 20
(PRIOR ART)

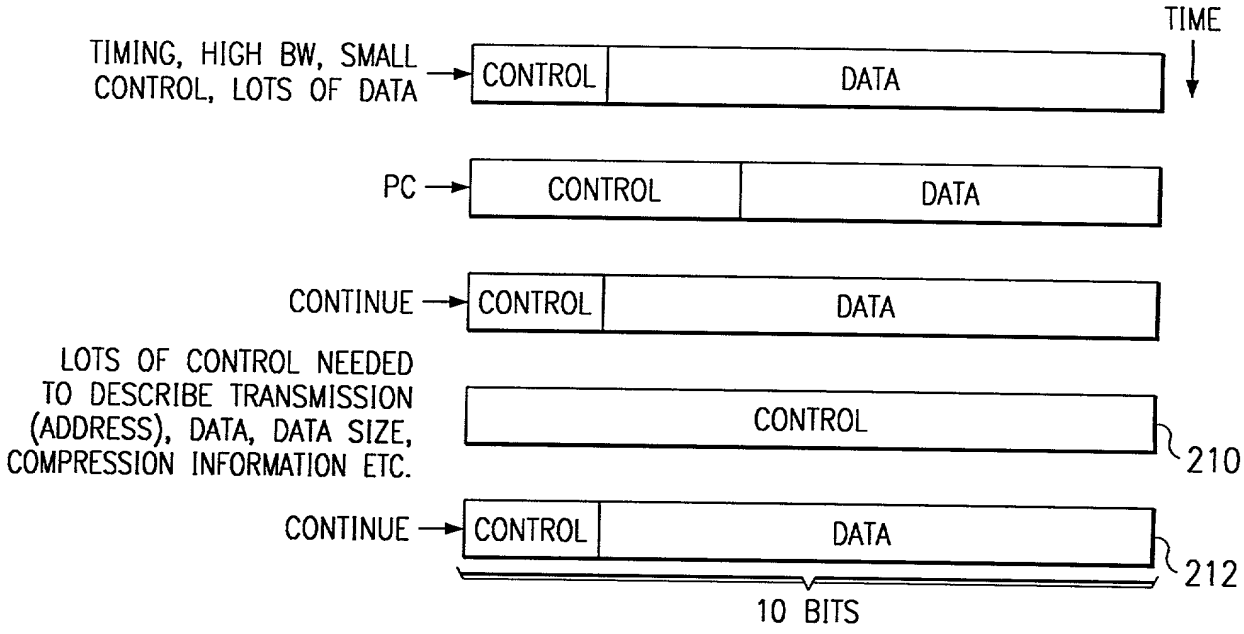


FIG. 21

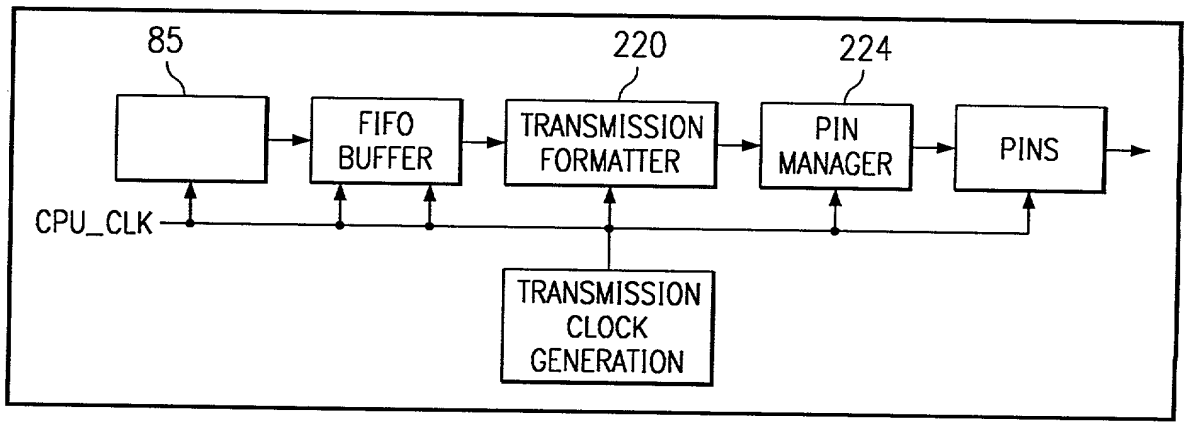


FIG. 22

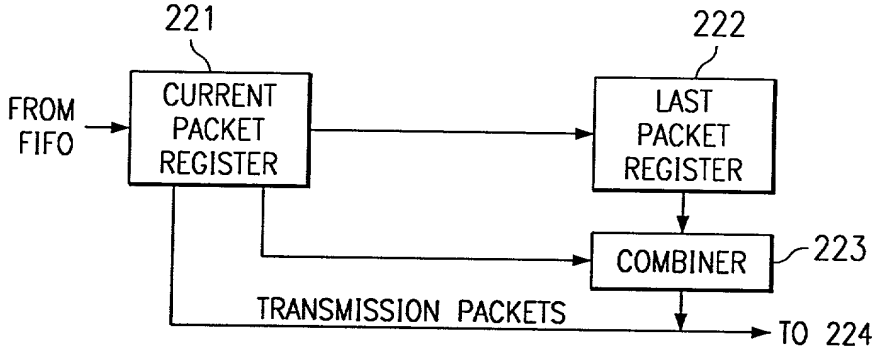


FIG. 22A

6 TRACE PACKETS TRANSMITTED AS 10 TRANSMISSION PACKETS									
10		10		10		10		10	10
6	6	6	6	6	6	6	6	6	6
TIME ⟶									

FIG. 23

10	10	10	10	10	10
12	12	12	12	12	

FIG. 23A

10	10	10	10	10	10	10	10
16	16	16	16	16			

FIG. 23B

REGISTER 221

REGISTER 222

#	CURRENT TRANSMISSION PACKET									#	INCOMPLETE TRANSMISSION PACKET								
0	9	8	7	6	5	4	3	2	1	0	EMPTY									
1	9	8	7	6	5	4	3	2	1	0	0	9	8	7	6	5	4	3	2	1	0
1	9	8	7	6	5	4	3	2	1	0	1	9	8	7	6	5	4	3	2	1	0
2	9	8	7	6	5	4	3	2	1	0	1	9	8	7	6	5	4	3	2	1	0
2	9	8	7	6	5	4	3	2	1	0	2	9	8	7	6	5	4	3	2	1	0
3	9	8	7	6	5	4	3	2	1	0	2	9	8	7	6	5	4	3	2	1	0

FIG. 24

221 222

	#	REGISTER										#	REGISTER									
	0	9	8	7	6	5	4	3	2	1	0	EMPTY										
	0	9	8	7	6	5	4	3	2	1	0	0	9	8	7	6	5	4	3	2	1	0
	0	9	8	7	6	5	4	3	2	1	0	0	9	8	7	6	5	4	3	2	1	0
	0	9	8	7	6	5	4	3	2	1	0	0	9	8	7	6	5	4	3	2	1	0
251	1	9	8	7	6	5	4	3	2	1	0	0	9	8	7	6	5	4	3	2	1	0
	1	9	8	7	6	5	4	3	2	1	0	1	9	8	7	6	5	4	3	2	1	0
	2	9	8	7	6	5	4	3	2	1	0	1	9	8	7	6	5	4	3	2	1	0

FIG. 25

221 222

	#	REGISTER										#	REGISTER										
	0	9	8	7	6	5	4	3	2	1	0	EMPTY											
	Z	–	–	Z	E	R	O	E	S	–	–	0	9	8	7	6	5	4	3	2	1	0	261
262	Z	–	–	Z	E	R	O	E	S	–	–	Z	–	–	Z	E	R	O	E	S	–	–	
	Z	–	–	Z	E	R	O	E	S	–	–	Z	–	–	Z	E	R	O	E	S	–	–	
263	1	9	8	7	6	5	4	3	2	1	0	Z	–	–	Z	E	R	O	E	S	–	–	
264	1	9	8	7	6	5	4	3	2	1	0	1	9	8	7	6	5	4	3	2	1	0	
	2	9	8	7	6	5	4	3	2	1	0	1	9	8	7	6	5	4	3	2	1	0	

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FIG. 26

221 222

	#	REGISTER										#	REGISTER									
	0	9	8	7	6	5	4	3	2	1	0	EMPTY										
	Z	–	–	Z	E	R	O	E	S	–	–	0	9	8	7	6	5	4	3	2	1	0
	Z	–	–	Z	E	R	O	E	S	–	–	Z	–	–	Z	E	R	O	E	S	–	–
	Z	–	–	Z	E	R	O	E	S	–	–	Z	–	–	Z	E	R	O	E	S	–	–
	Z	–	–	Z	E	R	O	E	S	–	–	Z	–	–	Z	E	R	O	E	S	–	–
	Z	–	–	Z	E	R	O	E	S	–	–	Z	–	–	Z	E	R	O	E	S	–	–
	Z	–	–	Z	E	R	O	E	S	–	–	Z	–	–	Z	E	R	O	E	S	–	–
	Z	–	–	Z	E	R	O	E	S	–	–	Z	–	–	Z	E	R	O	E	S	–	–
271	1	9	8	7	6	5	4	3	2	1	0	Z	–	–	Z	E	R	O	E	S	–	–
	1	9	8	7	6	5	4	3	2	1	0	1	9	8	7	6	5	4	3	2	1	0
	2	9	8	7	6	5	4	3	2	1	0	2	9	8	7	6	5	4	3	2	1	0

FIG. 27